Booster Beam Position Monitor System

System description

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Booster Beam Position Monitor system controls

Introduction

There are 24 vertical and 24 horizontal Beam Position Monitors (BPMs) located in the Booster ring. Each BPM consists of two opposing plates within the vacuum chamber. Each plate generates a signal when the beam passes by. The signal from each plate is wired to building 914 with coaxial cable where the signal processing circuitry generates the position and intensity of the Booster beam. This information is then sent to the control equipment for further processing by the accelerator control system.

Position processing unit

The signals from the Booster BPMs are input to an RF group designed "remote position-processing unit". This device converts the signals to sum and difference information. The sum of the plate signals is the beam intensity and the difference is the beam position. The position- processing unit also converts the voltage domain signals to frequency domain signals in the range of 20 to 40 Mhz. 20 Mhz signifies that the beam is positioned towards the inside (Horizontal BPM) of the beam pipe or towards the bottom (Vertical BPM) of the beam pipe and 40Mhz signifies that the beam is positioned towards the outside or top of the beam pipe. 30 Mhz signifies that the beam is at the center of the beam pipe for both axis. As stated above the system also generates beam intensity information. In this case 20Mhz represents very low intensity and 40 Mhz represents high intensity. For each 3Mhz change the intensity is increased by a factor of 10. The intensity information is a relative measure of the beam intensity.

The "position - processing unit" finally converts the frequency domain signals to optical signals that are transmitted over multimode fibers operating at 850nm to the accelerator control stations in Rack 5728.

Booster BPM Controls

. The first station, CST.914.MUXBPM, in Rack 5728 is a 9U chassis containing the Receiver/Multiplexor modules. These modules convert the optical signals from the position-processing units back to electrical signals. Each module can also route any eight of the sixteen input signals to a custom bus on the P2 connector thus forming a 16X8 Multiplexor.

This chassis (see specification ACC/96-1 – 9U Control Chassis) has three DIN connectors instead of the usual two for standard VME chassis'. The first 4 slots of the chassis are 6U slots and have the full VME bus structure. That is, P1 and the center row of P2 are used for VME. The remaining slots (5-21) are 9U slots and incorporate only the P1 connector for VME. Therefore, these slots can only support 16 bit addressing and 16 bit data transfers. The custom bus structure described above is on Row B of the P2 connectors in slots 5-21 and its function is to route frequency domain signals from each of the Receiver/Multiplexor modules to the V122 – fiber optic transmitter. The P3 connector in slots 5-21 is not bused and is used to route the frequency domain signals to the T121 transition modules located in the rear of the chassis.

CST.914.MUXBPM Hardware

See block diagram on page 6

This chassis contains the following modules

- A Motorola 2100 FEC
- A memory card
- A V108
- 6 V221 receiver/mux boards and 6 T121 transition modules
- 1 V122 fiber optic transmitter module

The V221s are 9U boards and have three connectors in the rear. They are functionally equivalent to the V121 boards (see V121 on the Controls Hardware WEB page) used in the AGS BPM system. However, the V221s have LVDT outputs on the P3 connector to handle the higher frequencies at which the Booster system operates (the AGS system uses frequencies of 8Mhz to 10Mhz).

The V221s receive the optical signals from the position-processing modules on the front panel and convert the signals back to electrical. The signals are buffered and routed via the P3 connector to the T121 transition modules. The signals are then sent over shielded ribbon cable to T121 transition modules in CST.914.BPM.

The V221 can output any eight of its sixteen inputs to a bus on the P2 connector to the V122 board, which converts the signals back to optical signals. The six V221's thus form a 96X8 mux. The V122 transmits the selected signals on the P2 bus on fiber to building 911B where they are converted back to a +/- 10 Volt analog signal (+/-10V is into high impedance. Into 50 Ohms the signal is +/_ 1 Volt). At the time this was written the device to convert the optical signals to analog voltage signals was not installed. The selection of signals is made through application software. The application software also provides logic that prevents two or more V221s from routing signals on the same bus line.

The V221s are addressed starting at 0xD000 for the first card through 0xd500 for the sixth card. See the "Hardware Configuration Data Base" for V221 jumpers

The second station, CST.914.BPM, in rack 5728 is a standard 6U VME chassis. The scaler modules count the frequency domain signals for the period of time defined by the V102 generated "read gate" converting the signal back to a scalar that represents beam

position and beam intensity. The data is buffered in memory on the V116 until the application software reads the memory after each booster cycle.

CST.914.BPM Hardware

See block diagram on page 5

This 6U VME chassis contains the following modules

- A Motorola 2100 FEC
- A memory card
- A V108
- A V102
- A V194
- 6 V116-2 scaler boards and 6 T121 transition modules

Each of the V116-2 (see the V116 write up on the Controls Hardware WEB page) scaler boards had sixteen inputs. The frequency domain signals are input to the V116 P2 connectors via T121 transition modules. The V116-2 differs from the V116-1 by having LVDT receivers on the P2 inputs to accommodate the 20 – 40 Mhz frequency range of the Booster BPM system.

There are two control inputs to the V116 board. The first is the "BPM read gate" (Gate input on the front panel) and is (at the time this was written) generated by decoding the event BMD.PUE_RD.RT (code 0x6a) in the V102. The V102 pulse width (a programmable variable) determines how long the scalers count. The V116 counts the frequency domain signals for the duration of the read gate and then stores the results in FIFO memory. BMD.PUE_RD.RT can be scheduled up to 16 times per cycle. The decoded read gate signal has to be a low going pulse. The V116 is capable of storing up to 215 readings per Channel.

The second control input is the input that erases the data in the FIFO and sets the time stamp counter back to zero (The T0 input on the front panel). The event code Bt0 (0x0a), decoded in the V102 is used (at the time this was written) for this function. The signal produced must also be a low going pulse to the V116. The data stored in the FIFO during the previous cycle must be read out of the V116 memory before the BT0 event occurs or the data for the cycle will be lost.

Both outputs of the V102 (gate and T0) are input to a V194 where the signals are fanned out to the V116s.

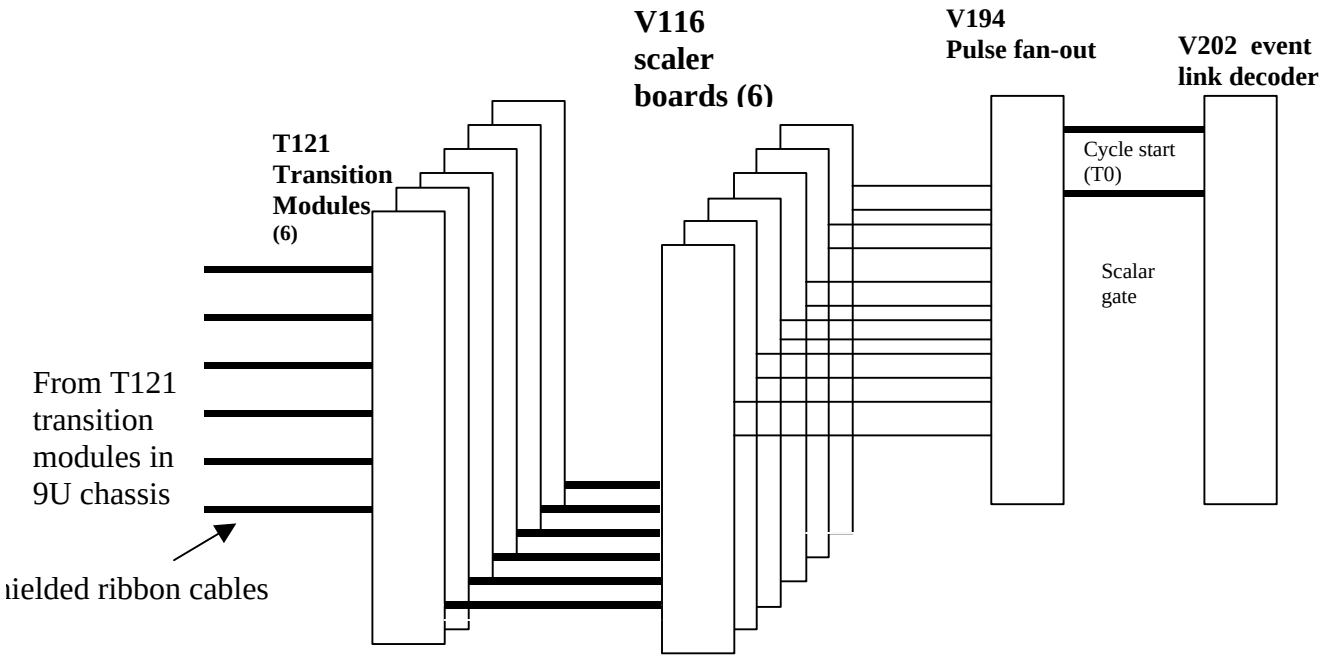
The six V116 boards are addressed as the first six boards in the V116 specification.

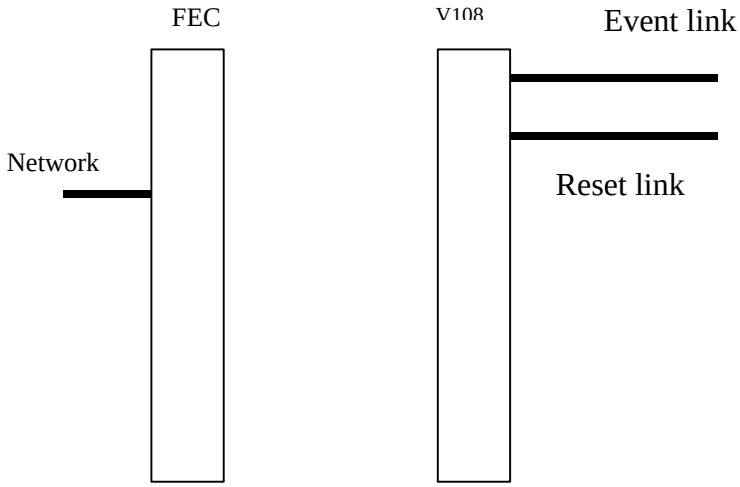
The V116s are configured to have the inputs on the rear connector.

As stated above, the V102 outputs used for the Gate and T0 inputs to the V116 must be low going.

See the "Hardware Configuration Data Base" for V116 jumpers

CST.914.BPM





Booster BPM 6U chassis

Scaler boards V216& T121 trans. Modules - 6 ea.

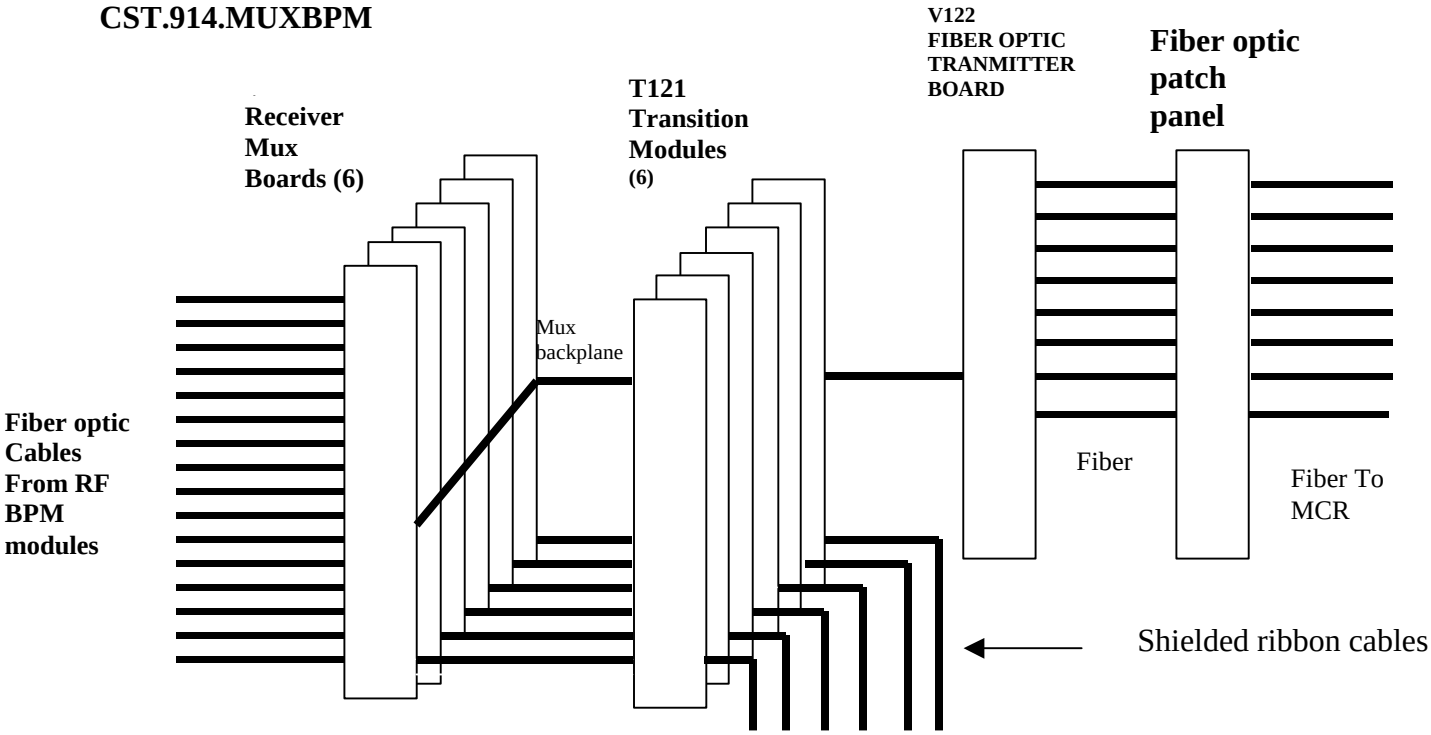
V102 event link decoder board

V194 Pulse fan-out

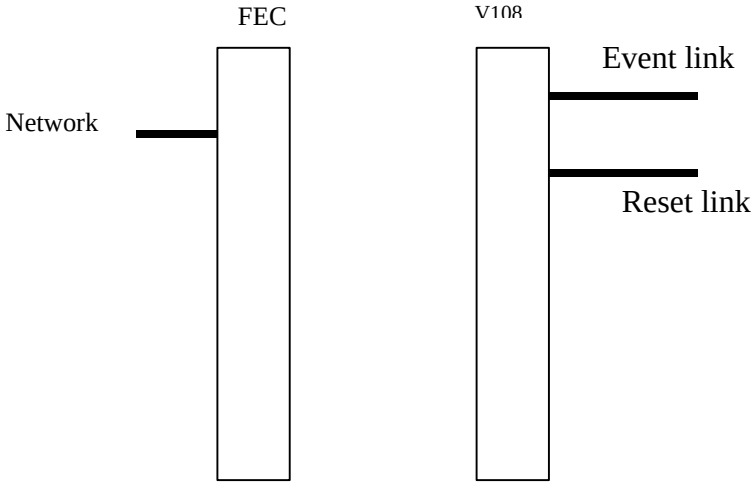
FEC

V108

CST.914.MUXBPM



To scalars in 6U VME chassis via
T121 modules for scaler inputs



Booster BPM 9U chassis

Fiber optic receiver/ mux boards V221& T121 trans. Modules - 6 ea.

Mux fiber optic transmitter board – V122

FEC

V108